REMARKS

Examiner Arora is thanked for the thorough examination and search of the subject patent application.

Claims 1, 4, 7, 9-12, 15, 17-19, 21, 22, 25, 27, 29, 30, 91, 96-99 and 101-103 are pending; Claims 9, 15, 97, 99, 102 and 103 have been currently amended; Claims 4 has been withdrawn; Claims 29 and 30 have been withdrawn and currently amended; Claims 2, 3, 5, 6, 8, 13, 14, 16, 20, 23, 24, 26, 28, 31-90, 92-95, 100 and 104-107 have been canceled. No new matter is believed to have been added.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 1, 4, 7, 91, 96 and 97

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As previously presented, independent Claim 1 is recited below:

1. An integrated circuit chip with multiple wirebonds, comprising:

a semiconductor substrate;

a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a second contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over said first contact pad and exposes said first contact pad, and wherein a second opening in said passivation layer is over said second contact pad and exposes said second contact pad;

a power metal structure over said passivation layer and on said first contact pad, wherein said power metal structure is connected to said first contact pad through said first opening, wherein said power metal structure comprises a copper layer, and wherein one of said multiple wirebonds is bonded on said power metal structure;

a ground metal structure over said passivation layer and on said second contact pad, wherein said ground metal structure is connected to said second contact pad through said second opening, wherein said ground metal structure comprises a copper layer, and wherein another one of said multiple wirebonds is bonded on said ground metal structure;

a capacitor over said passivation layer and directly over said first contact pad exposed by said first opening;

a first solder connection connecting said capacitor to said power metal structure; and

a second solder connection connecting said capacitor to said ground metal structure.

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Reconsiderations of Claims 1, 7 and 91 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. (U.S. Pat. No. 5,629,240), of Claim 96 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. in view of Efland et al. (U.S. Pat. No. 6,020,640), and of Claim 97 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. in view of Greer (U.S. Pat. No. 6,451,681) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip claimed in Claim 1 patentably distinguishes over the citation by Malladi et al. (U.S. Pat. No. 5,629,240).

The Examiner considers that "Malladi does not teach that the said power metal structure and the said ground metal structure each comprise a "copper" layer. However, the use of copper for metallization, including power or ground metallization layer, is well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi so that the said power metal structure and the said ground metal structure each comprise a copper layer. The ordinary artisan would be motivated to modify Malladi at least for the purpose of using a high thermal and electrical conductivity metal for the power and ground metal structure for efficient power distribution with minimal losses." ~ *See line 15 of page 6 through line 2 of page 7, in the last Office Action mailed Apr. 1, 2008* ~

Applicant respectfully traverse the Examiner's opinion because it would not have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi et al. so that power and ground metal structures having a capacitor formed thereover using a solder comprise a copper layer. Malladi et al. teach that the power or ground metal structure 68 or 66 is formed of platinum, tungsten, aluminum or silver. ~ *See col. 5, lines 32-47* ~ However, Malladi et al. fail to teach, hint or suggest that the power or ground metal structure 68 or 66 may comprise a copper layer, as currently claimed in Claim 1. Furthermore, the Examiner fails to show any evidence that the power or ground metal structure 68 or 66 having a capacitor formed thereover

using a solder may comprise a copper layer. If the Examiner considers that the claimed subject matter that "a power or ground metal structure having a capacitor formed thereover using a solder comprises a copper layer" is anticipated, showing an evidence is respectfully requested.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 1 is respectfully requested.

Applicants respectfully submit independent Claim 1 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 4, 7, 91, 96 and 97 patentably define over the prior art as well.

Response to Claims 9-12, 98 and 99

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As currently amended, independent Claim 9 is recited below:

9. An integrated circuit chip comprising:
a semiconductor substrate;
a transistor in and on said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a first contact pad over said semiconductor substrate;
a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over said first contact pad and exposes said first contact pad, and wherein said passivation layer comprises a nitride;
a second contact pad connected to said first contact pad through said first opening, wherein the position of said second contact pad from a top perspective view

is different from that of said first contact pad, and wherein said second contact pad comprises a gold layer with a thickness greater than 1 micrometer;

a capacitor over said passivation layer and over said second contact pad;

a solder connection between said capacitor and said second contact pad, wherein said solder connection connects said capacitor to said second contact pad; and

an additional metal layer between said solder connection and said second contact pad.

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Reconsiderations of Claims 9-12, 98 and 99 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. (U.S. Pat. No. 5,629,240) in view of Master (U.S. Pub. No. 2003/0037959) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip claimed in Claim 9 patentably distinguishes over the citation by Malladi et al. (U.S. Pat. No. 5,629,240) in view of Master (U.S. Pub. No. 2003/0037959).

The Examiner considers that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi such that said second contact pad comprises a gold layer with a thickness greater than 1 micrometer and there is an additional metal layer between said solder connection and said second contact pad. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing a gold layer that has optimal thickness for its intended purpose (such as providing resistance against corrosion, increasing wettability, etc.) for the given design and providing the additional metal layer to provide a barrier layer between the solder and

the underlying device. *~ See lines 11-19 on page 10, in the last Office Action mailed Apr. 1, 2008 ~*

Applicant respectfully traverse the Examiner's opinion because it would not have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi et al. in view of Master such that a contact pad having a capacitor formed thereover using a solder comprises a gold layer with a thickness greater than 1 micrometer.

In paragraph [0027] in Master's teaching, Master teaches that "In the flip chip process, solder bumps are formed over bonding pads of a semiconductor device. Metal layers are provided between the solder bump and bonding pad of the device, i.e. under bump metallurgy, to promote adhesion of the solder, ensure wettability by the solder and provide a barrier between the solder and the underlying device. Examples of under bump metallurgy include one or more layers of chrome, copper and gold. Other examples of metal layers used in under bump metallurgy include one or more layers of nickel and gold; one or more layers of titanium and copper; or alloys thereof."

However, Malladi et al.'s forming a capacitor over a chip is believed to be not within the scope of the flip-chip process, as above recited by Master. Therefore, Master's under bump metallurgy is believed to be non-analogous to Malladi et al.'s conductive elements 66 and 68. The claimed subject matter that a contact pad having a capacitor formed

thereover using a solder comprises a gold layer having a thickness greater than 1 micrometer, as currently claimed in Claim 9, is believed not to be obvious over Malladi et al. in view of Master. Furthermore, the claimed subject matter that an additional metal layer is between a solder connection under a capacitor and a relocated contact pad, as currently claimed in Claim 9, is believed not to be obvious over Malladi et al. in view of Master.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 9 is respectfully requested.

Applicants respectfully submit independent Claim 1 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 10-12, 98 and 99 patentably define over the prior art as well.

Response to Claims 15, 17-19, 21, 22, 25, 27, 29, 30 and 101-103

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As currently amended, independent Claim 15 is recited below:

15. An integrated circuit chip with a wirebond, comprising:
a semiconductor substrate;
a transistor in and on said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over said first contact pad and exposes said first contact pad;

a second contact pad connected to said first contact pad through said first opening;

a third contact pad connected to said first contact pad through said first opening and connected to said second contact pad, wherein the position of said third contact pad from a top perspective view is different from that of said first contact pad, and wherein said wirebond is bonded on said third contact pad;

a first polymer layer over said passivation layer, wherein a second opening in said first polymer layer is over said second contact pad and exposes said second contact pad;

a capacitor over said first polymer layer and over said second contact pad; and

a solder connection between said second contact pad and said capacitor, wherein said solder connection connects said capacitor to said second contact pad.

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Reconsiderations of Claims 15, 19, 21, 22, 25 and 101 rejected under 35 U.S.C. 102(b) as being anticipated by Malladi et al. (U.S. Pat. No. 5,629,240), of Claims 17, 18, 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al., and of Claims 31, 102 and 103 rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al. in view of Greer (U.S. Pat. No. 6,451,681) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip claimed in currently-amended Claim 15 patentably distinguishes over the citation by Malladi et al. (U.S. Pat. No. 5,629,240).

The Examiner considers that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Malladi in view of Greer so that there

is a polymer layer over said passivation, wherein a second opening in said polymer layer is over said second contact pad and exposes said second contact pad. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing an additional protection layer over the metallization but providing openings in the polymer layer (just like openings in passivation layer) as required to form interconnections." ~ *See lines 10-17 of page 12, in the last Office Action mailed Apr. 1, 2008* ~

Applicant respectfully traverse the Examiner's opinion because it would not have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi et al. in view of Greer so that a capacitor can be over a polymer layer and can be connected to a contact pad, exposed by an opening in the polymer layer, which is connected to another contact pad exposed by an opening in a passivation layer.

Greer teaches that both an opening in a passivation layer 300, 500 or 704 and an opening in a polymer layer 302, 502 or 706 expose a same contact pad 312, 124 or 716. ~ *See Figs. 3-7* ~ However, Greer fails to teach, hint or suggest that the opening in the passivation layer 300, 500 or 704 and the opening in the polymer layer 302, 502 or 706 may expose different contact pads, as currently claimed in Claim 15. Therefore, the claimed subject matter that a capacitor is over a polymer layer and is connected to a contact pad, exposed by an opening in the polymer layer, which is connected to another contact pad exposed by an opening in a passivation layer, as currently claimed in Claim 15, is believed not to be obvious over Malladi et al. in view of Greer.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 15 is respectfully requested.

Applicants respectfully submit independent Claim 15 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 17-19, 21, 22, 25, 27, 29, 30 and 101-103 patentably define over the prior art as well.

Conclusion

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Arora not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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